

Atty. Docket No. 02986.P035

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of:

John M. Beardslee, et al.

Application No. 09/724,585

Filed: November 28, 2000

For: METHOD AND SYSTEM FOR
DEBUGGING AN ELECTRONIC SYSTEM

Examiner: Thangavelu, K.

Art Unit: 2123

Confirmation No. 7620

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

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Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

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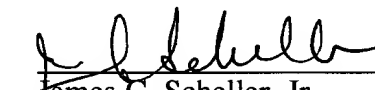
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 8/16, 2005


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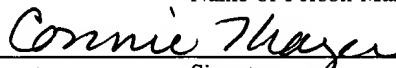
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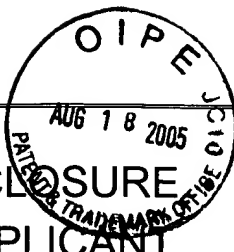
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			Filing Date	11/28/2000	
			First Named Inventor:	John M. Beardslee	
			Art Unit	2123	
Examiner Name	Thangavelu, K.				
Attorney Docket No.	02986.P035				
Sheet	1	of	7		

U.S. PATENT DOCUMENTS						
Exmnr Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
		US- 6,587,995	B1	07/01/2003	Duboc et al.	
		US- 6,779,145	B1	08/17/2004	Edwards et al.	
		US- 6,785,854	B1	08/31/2004	Jaramillo et al.	
		US- 6,789,217	B2	09/07/2004	Slaugh et al.	
		US- 6,791,352	B2	09/14/2004	Verdoorn et al.	
		US- 6,795,963	B1	09/21/2004	Andersen et al.	
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FOREIGN PATENT DOCUMENTS								
Exmnr Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
		WIPO	00/043884	A1	07/27/2000	Wenzel et al.		
		WIPO	01/063434	A1	08/30/2001	Barry		
		WIPO	01/071876	A1	09/27/2001	Ricchetti et al.		

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		US- 6,895,365	B2	05/17/2005	Voorhees et al.	
		US- 6,895,372	B1	05/17/2005	Knebel et al.	
		US- 6,904,577	B2	06/07/2005	Schubert et al.	
		US- 2004/0111252	A1	06/10/2004	Burgun et al.	
		US- 2004/0181385	A1	09/16/2004	Milne et al.	
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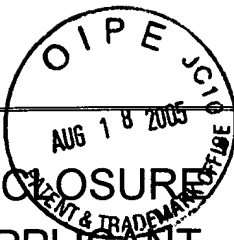
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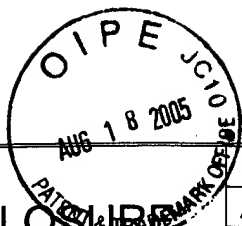
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		Ableidinger et al., "Multi-Core Embedded Debug for Structured ASIC Systems", DesignCon 2004, February 2004, 23 pgs.	
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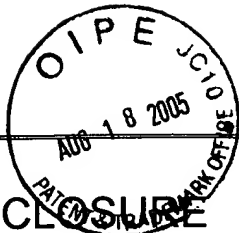
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		First Silicon Solutions, Inc., "Technical Data for ISA-ARM System Analyzer for ARM Processors and Cores", http://www.fs2.com , June 2005, 2 pgs.	
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		First Silicon Solutions, Inc., "Technical Data for Logic Navigator System for Atmel FPGA Devices", http://www.fs2.com , June 2005, 3 pgs.	

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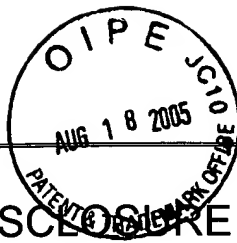
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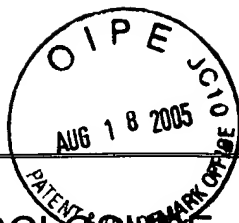
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		S2C Inc., "IP Porter Introduction", http://www.s2cinc.com/aaipi3.asp , June 2005, 9 pgs.			
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		Xilinx, Inc., "ChipScope Pro Software and Cores User Guide", UG029, Version v7.1, February 2005, 122 pgs.	
		Yang et al., "Extraction Error Modeling and Automated Model Debugging in High-Performance Low Power Custom Designs", Date Conference 2005, March 2005, 6 pgs.	

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